What Is Claimed Is:

1. A method for manufacturing a semiconductor device comprising:

forming a tunnel oxide film on a silicon substrate where a predetermined substructure is formed;

forming a particulate layer on the tunnel oxide film layer;

sequentially forming a control oxide film layer and a control gate layer on the particulate layer; and

forming a dual gate structure by patterning the control gate layer, the control oxide film layer, the particulate layer and the tunnel oxide film layer into a predetermined shape.

2. The method of claim 1, wherein the particulate layer comprises silicon.

3. The method of claim 1, wherein the particulate layer comprises silicon-germanium.

4. The method of claim 1, wherein the particulate layer is formed with a particle size of less than or about 60 nm in diameter density ranging from about 10^{11} to about 10^{12} particles per cm^2.

5. The method of claim 1, wherein the particulate layer has a particle density ranging from about 10^{11} to about 10^{12} particles per cm^2.

6. The method of claim 1, wherein the particulate layer forms a floating gate of a dual gate structure.

7. The method of claim 1, wherein the tunnel oxide film comprises an oxide film having a high dielectric constant of Ta_2O_5, HfO_2, ZrO_2 and mixtures thereof.

8. The method of claim 1, wherein the tunnel oxide layer is fabricated from a material selected from the group consisting of Ta_2O_5, HfO_2, ZrO_2 and mixtures thereof.

9. The method of claim 1, wherein the particulate layer is formed by using a rapid thermal chemical mechanical deposition (CVD) method.

10. The method of claim 1, wherein the control gate layer is formed from a silicon-germanium thin film doped in-situ.

11. The method of claim 3, wherein, in the step of forming a silicon-germanium particulate layer, the concentration is germanium is ranges from about 10 to about 20 wt%.

12. A method for manufacturing a dual gate structure of a semiconductor device comprising:

forming a tunnel oxide film on a silicon substrate, the tunnel oxide film having a roughed upper surface;

forming a particulate layer on the roughed upper surface of the tunnel oxide film layer, the particulate layer serving as a floating gate layer;

sequentially forming a control oxide film layer and a control gate layer on the floating gate layer; and

forming a dual gate structure by patterning the control gate layer, the control oxide film layer, the floating gate layer and the tunnel oxide film layer into a predetermined shape.

13. The method of claim 12, wherein the floating gate layer comprises silicon.

14. The method of claim 12, wherein the floating gate layer comprises silicon- germanium.

15. The method of claim 12, wherein the floating gate layer is formed with a particle diameter or cross-section having an upper limit of about 60 nm.

16. The method of claim 15, wherein the floating gate layer has a particle density ranging from about 10^{11} to about 10^{12} particles per cm^2.

17. The method of claim 12, wherein the tunnel oxide film layer comprises an oxide file having a high dielectric constant and is selected from the group consisting of Ta_2O_5, HfO_2, ZrO_2 and mixtures thereof.

18. The method of claim 12, wherein the floating gate layer is formed using a rapid thermal chemical mechanical deposition method.

19. The method of claim 12, wherein the control gate layer is formed from a silicon-germanium thin film doped in-situ.

20. The method of claim 14, wherein the concentration of germanium in the floating gate layer ranges from about 10 to about 20 wt%.